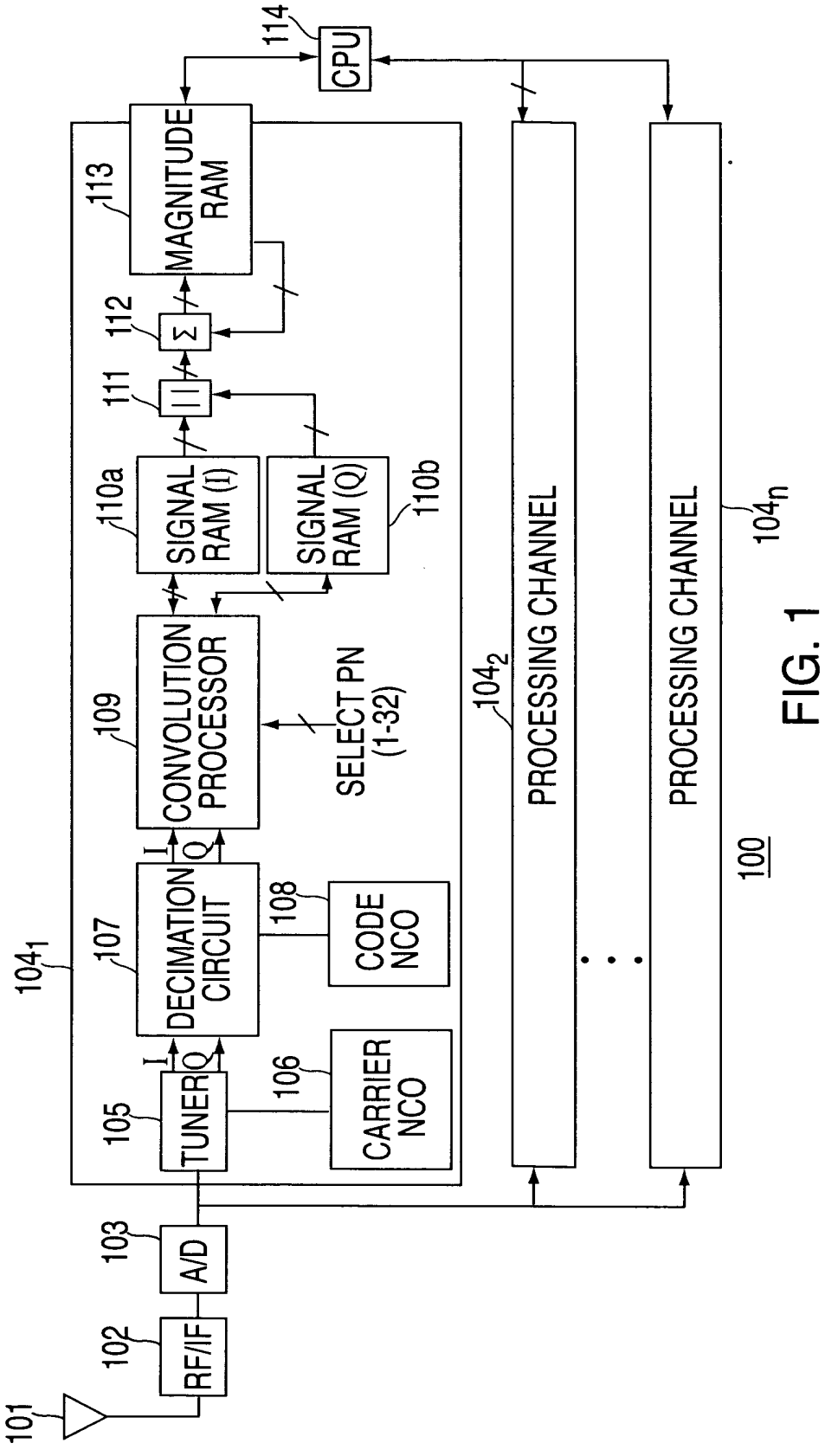
101
RF/IF
102
A/D
103
TUNER
I
Q
105
CARRIER NCO
106
DECIMATION CIRCUIT
I
Q
107
CODE NCO
108
CONVOLUTION PROCESSOR
109
SELECT PN (1-32)
SIGNAL RAM (I)
110a
SIGNAL RAM (Q)
110b
111
Σ
112
MAGNITUDE RAM
113
CPU
114
104_1
104_2
PROCESSING CHANNEL
PROCESSING CHANNEL
104_n
100

FIG. 1

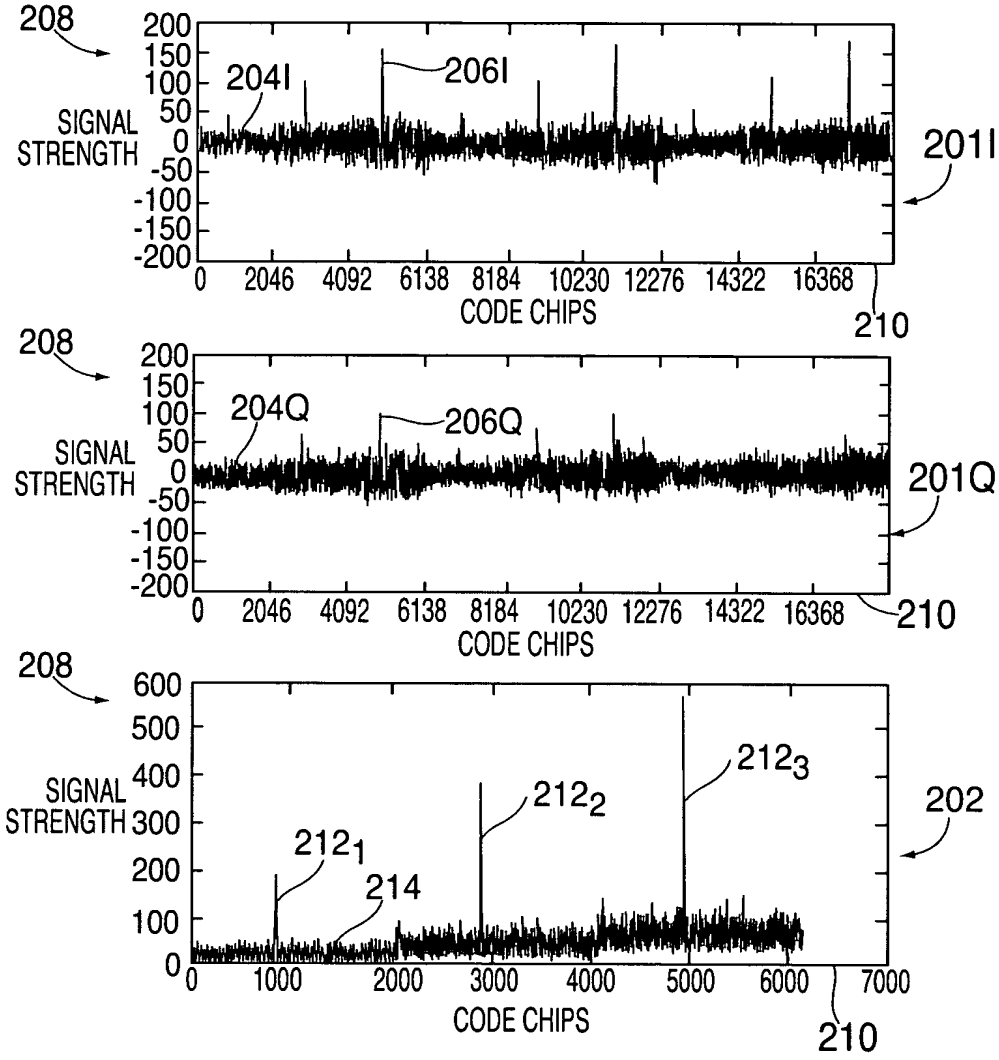
208
SIGNAL STRENGTH
200
150
100
50
0
-50
-100
-150
-200
2041
2061
2011
0 2046 4092 6138 8184 10230 12276 14322 16368
CODE CHIPS
210
208
SIGNAL STRENGTH
204Q
206Q
201Q
0 2046 4092 6138 8184 10230 12276 14322 16368
CODE CHIPS
210
208
SIGNAL STRENGTH
600
500
400
300
200
100
0
212_1
212_2
212_3
214
202
0 1000 2000 3000 4000 5000 6000 7000
CODE CHIPS
210

FIG. 2

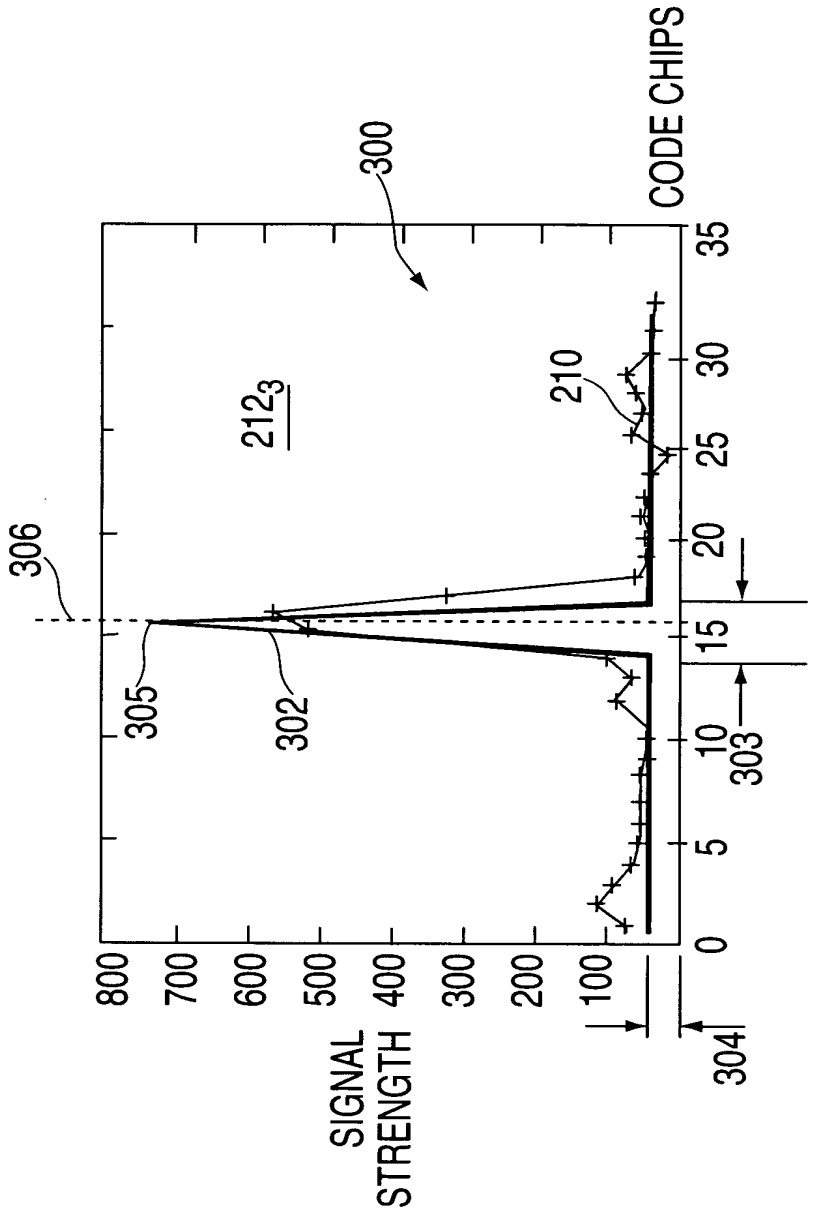
CODE CHIPS
SIGNAL STRENGTH
300
306
305
302
303
304
210
212_3
800
700
600
500
400
300
200
100
0
5
10
15
20
25
30
35

FIG. 3

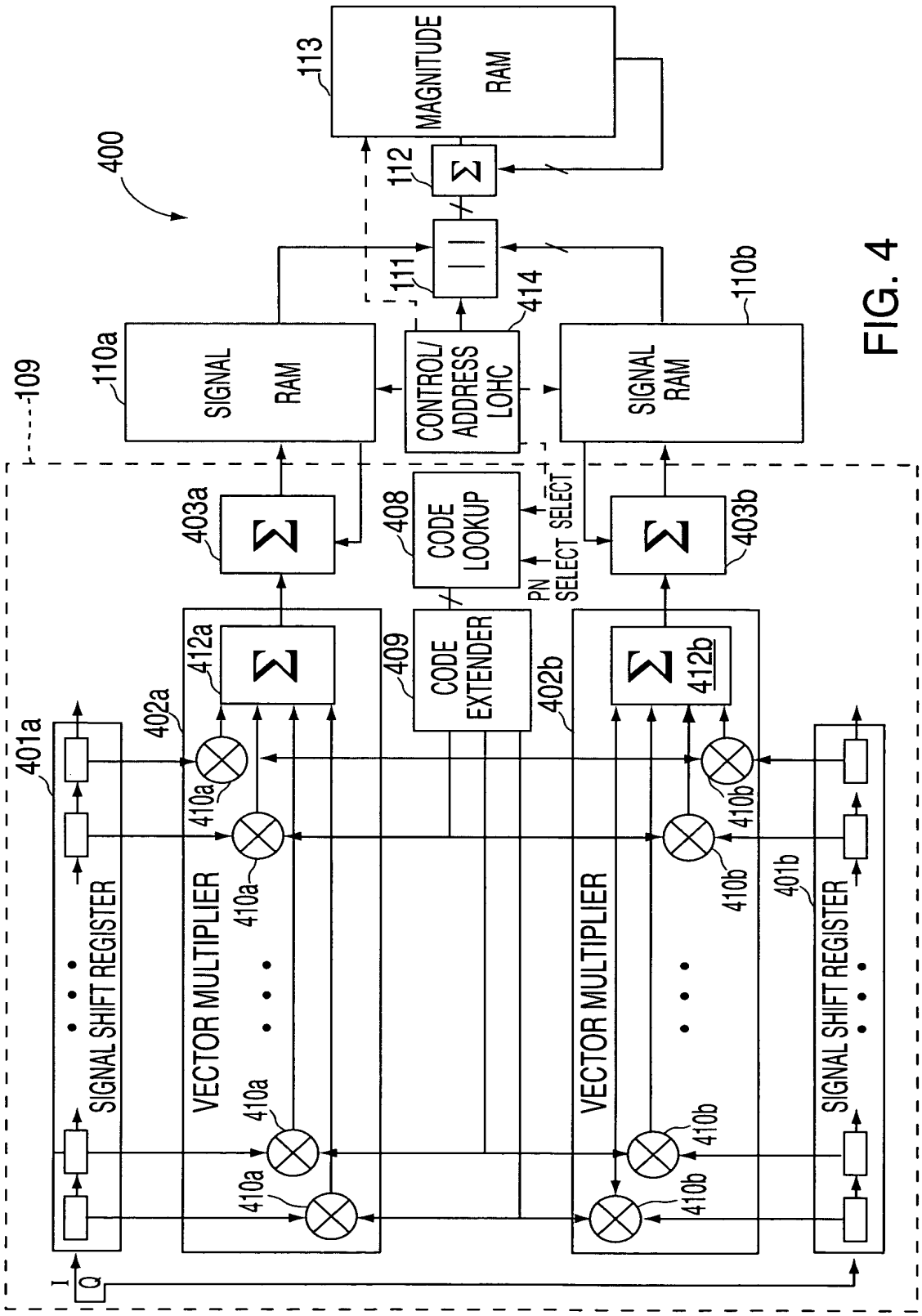
400
113
MAGNITUDE RAM
112
Σ
111
414
110a
SIGNAL RAM
CONTROL/ ADDRESS LOHC
110b
SIGNAL RAM
109
403a
Σ
408
CODE LOOKUP
PN SELECT
SELECT
403b
Σ
412a
Σ
409
CODE EXTENDER
402b
Σ
412b
402a
401a
SIGNAL SHIFT REGISTER
VECTOR MULTIPLIER
410a
410b
401b
SIGNAL SHIFT REGISTER
I
Q

FIG. 4

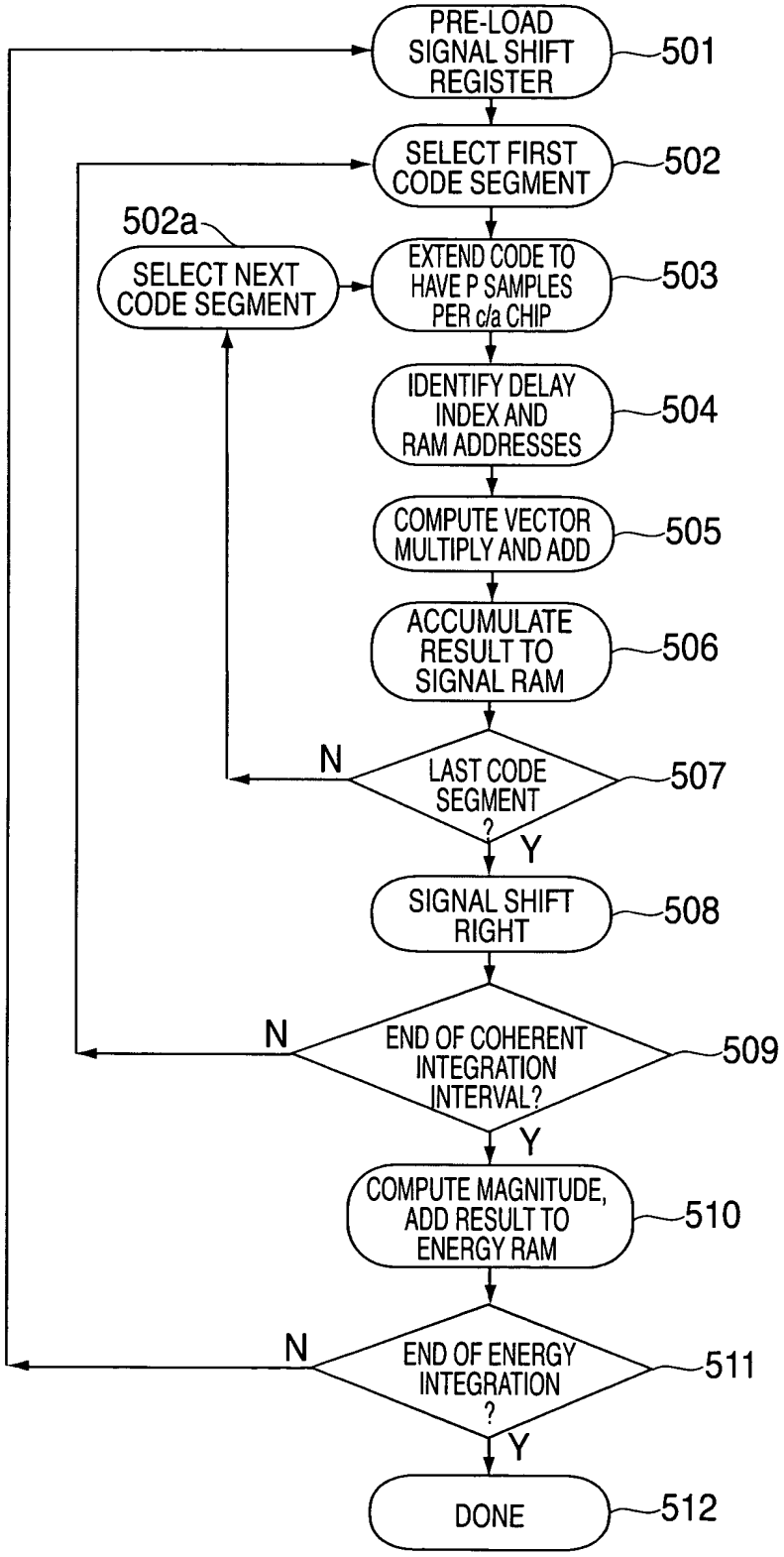
PRE-LOAD SIGNAL SHIFT REGISTER
501
SELECT FIRST CODE SEGMENT
502
502a
SELECT NEXT CODE SEGMENT
EXTEND CODE TO HAVE P SAMPLES PER c/a CHIP
503
IDENTIFY DELAY INDEX AND RAM ADDRESSES
504
COMPUTE VECTOR MULTIPLY AND ADD
505
ACCUMULATE RESULT TO SIGNAL RAM
506
N
LAST CODE SEGMENT ?
507
Y
SIGNAL SHIFT RIGHT
508
N
END OF COHERENT INTEGRATION INTERVAL?
509
Y
COMPUTE MAGNITUDE, ADD RESULT TO ENERGY RAM
510
N
END OF ENERGY INTEGRATION ?
511
Y
DONE
512

FIG. 5

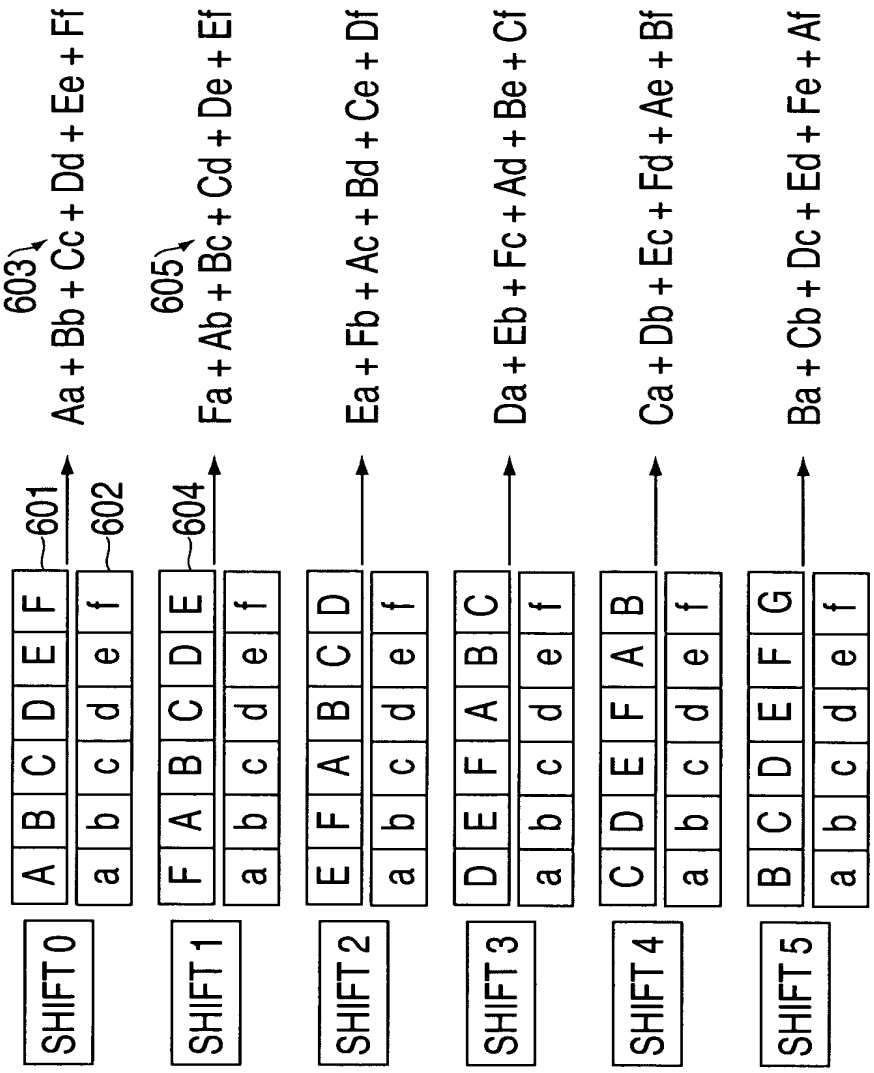

FIG. 6
(PRIOR ART)

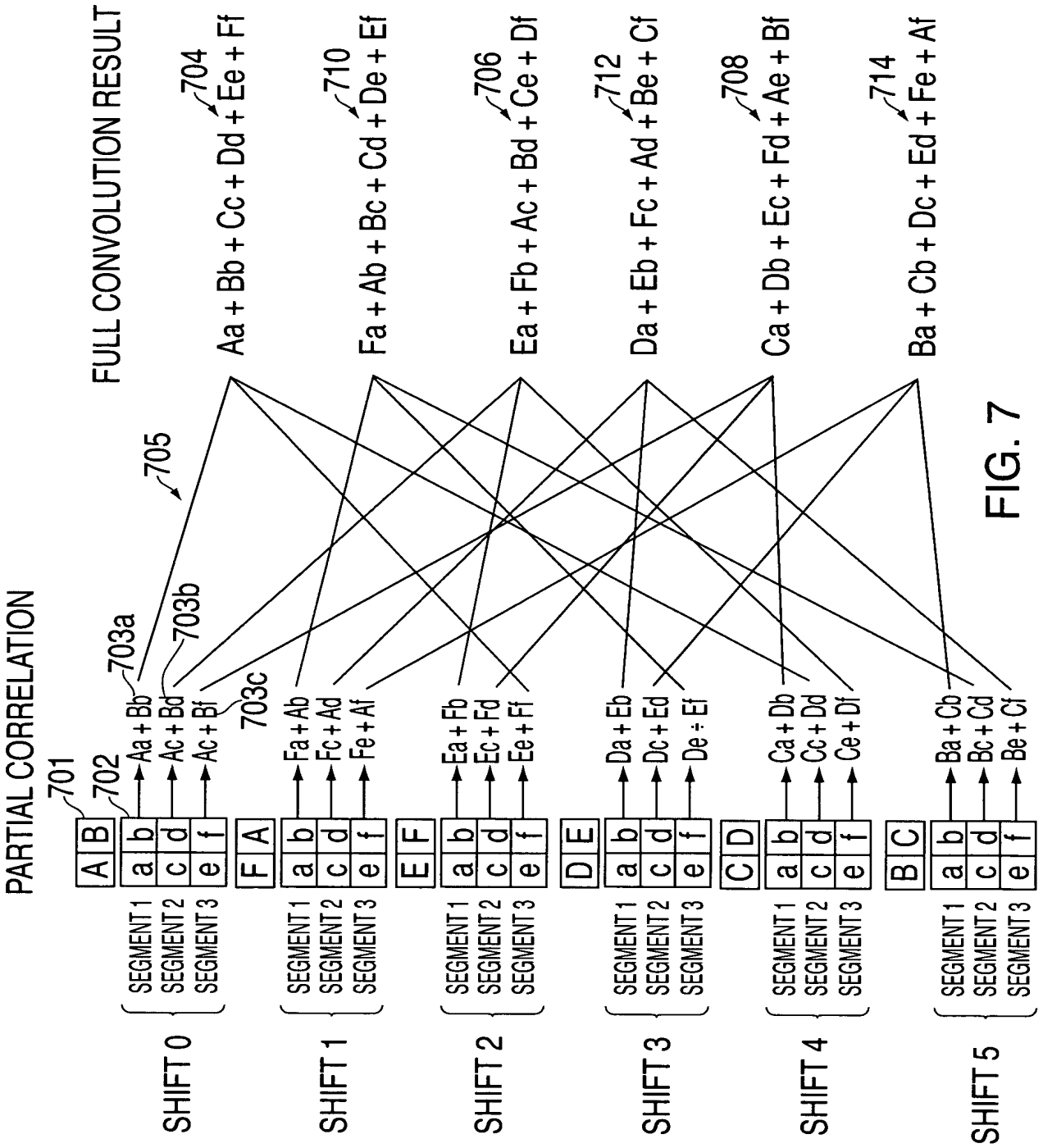
PARTIAL CORRELATION
701
FULL CONVOLUTION RESULT
705
703a
703b
703c
704
706
708
710
712
714
SHIFT 0
SHIFT 1
SHIFT 2
SHIFT 3
SHIFT 4
SHIFT 5
SEGMENT 1
SEGMENT 2
SEGMENT 3
Aa + Bb + Cc + Dd + Ee + Ff
Fa + Ab + Bc + Cd + De + Ef
Ea + Fb + Ac + Bd + Ce + Df
Da + Eb + Fc + Ad + Be + Cf
Ca + Db + Ec + Fd + Ae + Bf
Ba + Cb + Dc + Ed + Fe + Af

FIG. 7

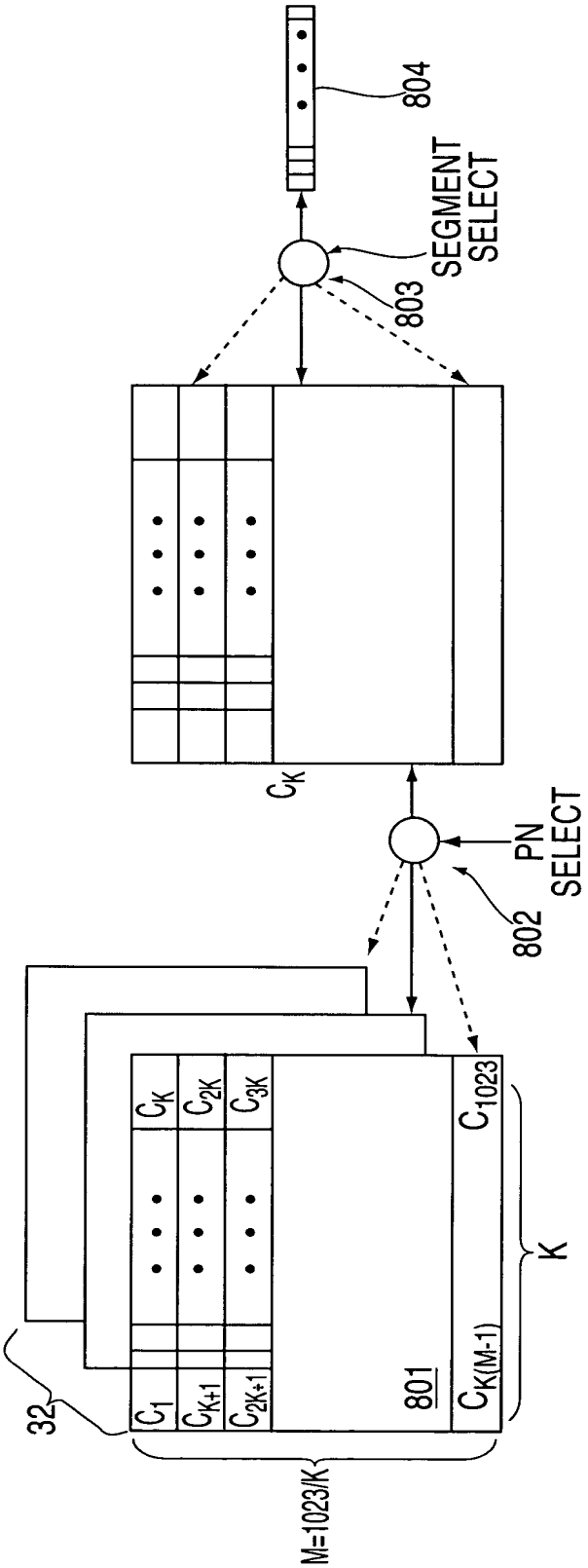
804
SEGMENT SELECT
803
C_K
PN SELECT
802
C_K
C_{2K}
C_{3K}
C_{1023}
K
801
32
C_1
C_{K+1}
C_{2K+1}
$C_{K(M-1)}$
M=1023/K

FIG. 8

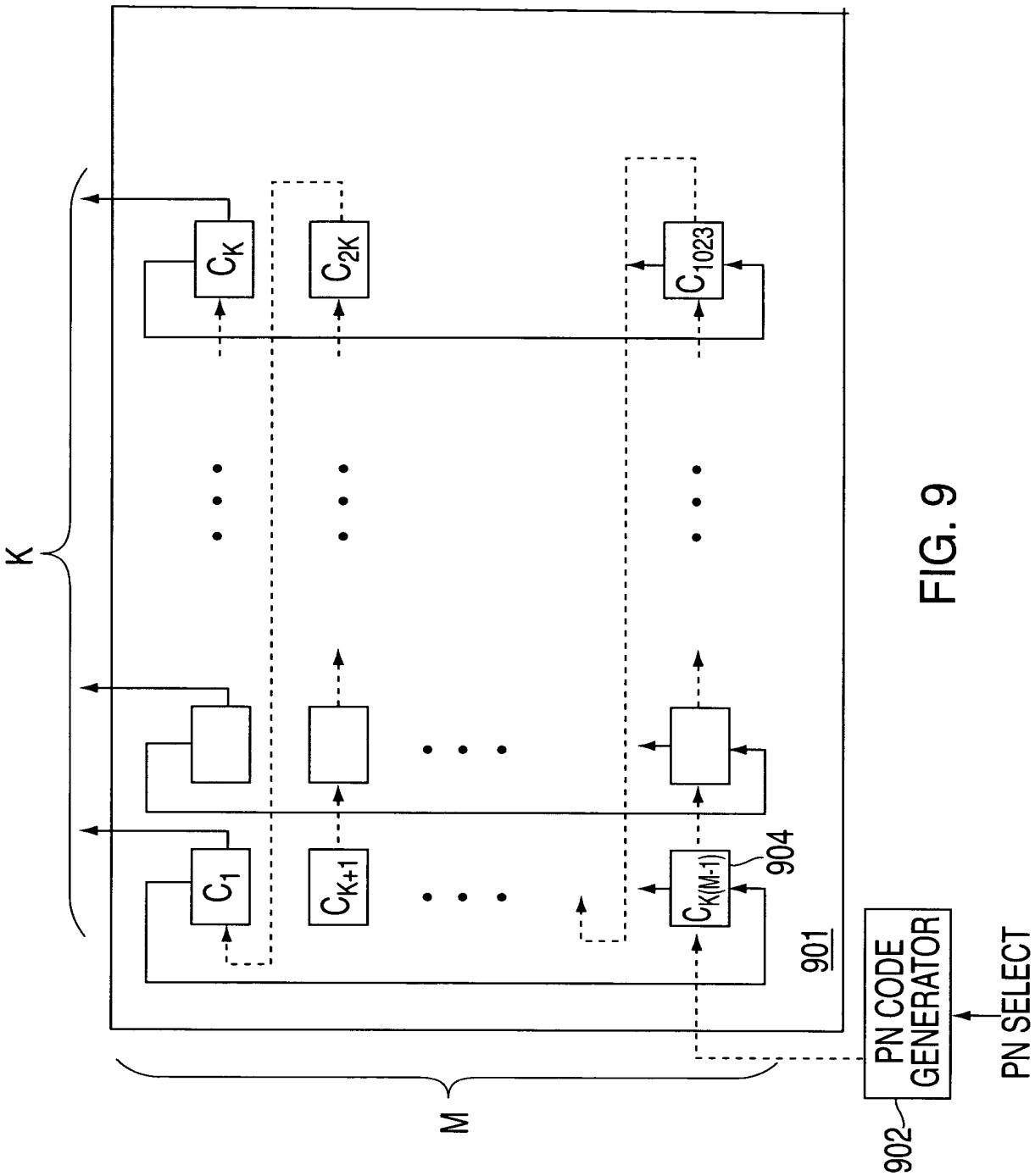
K
M
C_K
C_{2K}
C_{1023}
C_1
C_{K+1}
$C_{K(M-1)}$
904
901
PN CODE GENERATOR
902
PN SELECT

FIG. 9

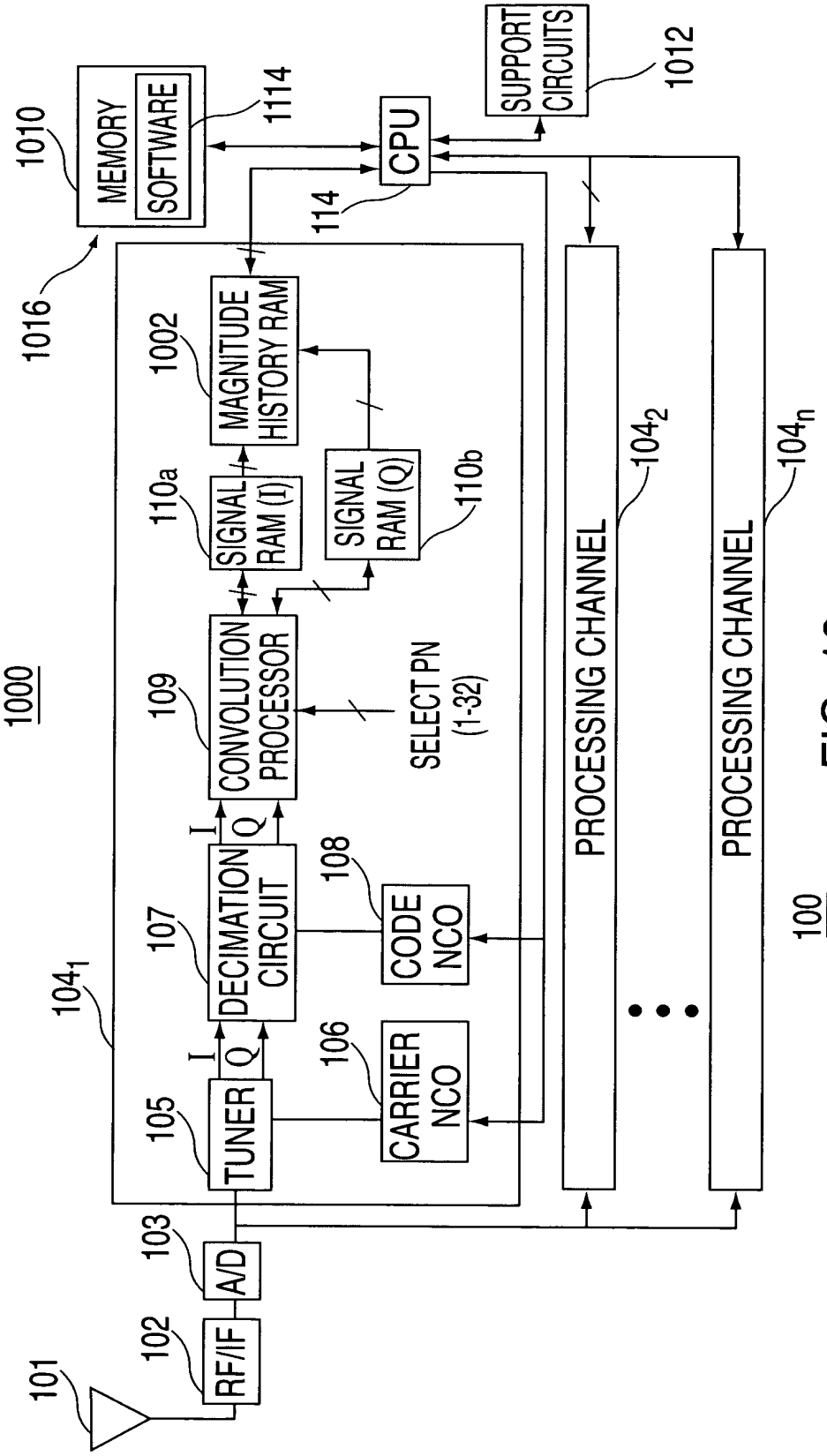
1000
1010
MEMORY
SOFTWARE
1114
1016
CPU
114
SUPPORT CIRCUITS
1012
1002
MAGNITUDE HISTORY RAM
110a
SIGNAL RAM (I)
SIGNAL RAM (Q)
110b
109
CONVOLUTION PROCESSOR
SELECT PN (1-32)
I
Q
DECIMATION CIRCUIT
107
108
CODE NCO
104_1
105
TUNER
106
CARRIER NCO
104_2
104_n
PROCESSING CHANNEL
PROCESSING CHANNEL
103
A/D
102
RF/IF
101
100

FIG. 10

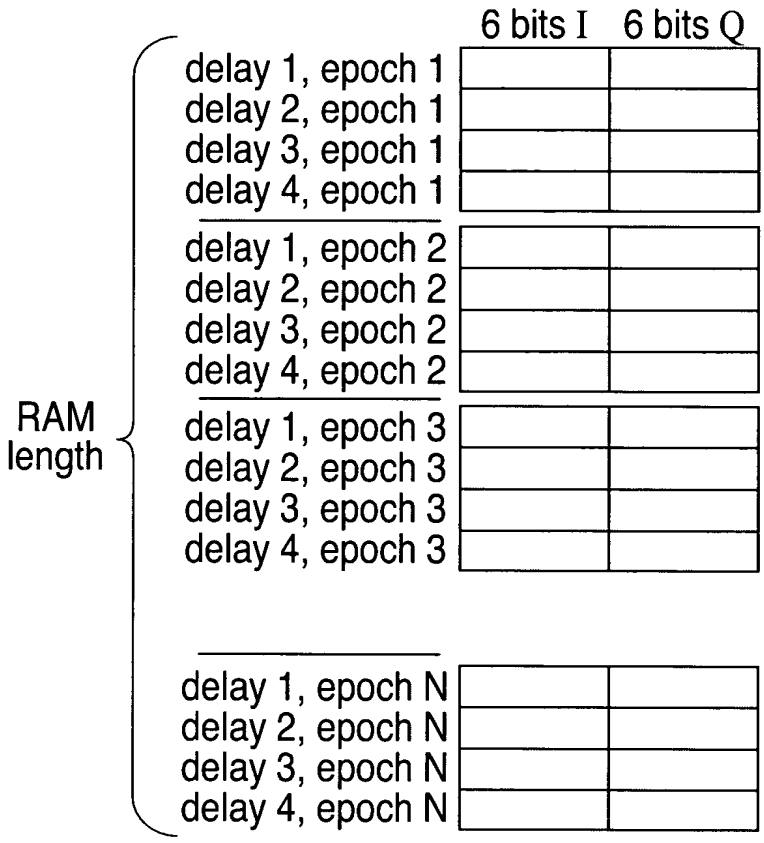
6 bits I
6 bits Q
RAM length
delay 1, epoch 1
delay 2, epoch 1
delay 3, epoch 1
delay 4, epoch 1
delay 1, epoch 2
delay 2, epoch 2
delay 3, epoch 2
delay 4, epoch 2
delay 1, epoch 3
delay 2, epoch 3
delay 3, epoch 3
delay 4, epoch 3
delay 1, epoch N
delay 2, epoch N
delay 3, epoch N
delay 4, epoch N

FIG. 11

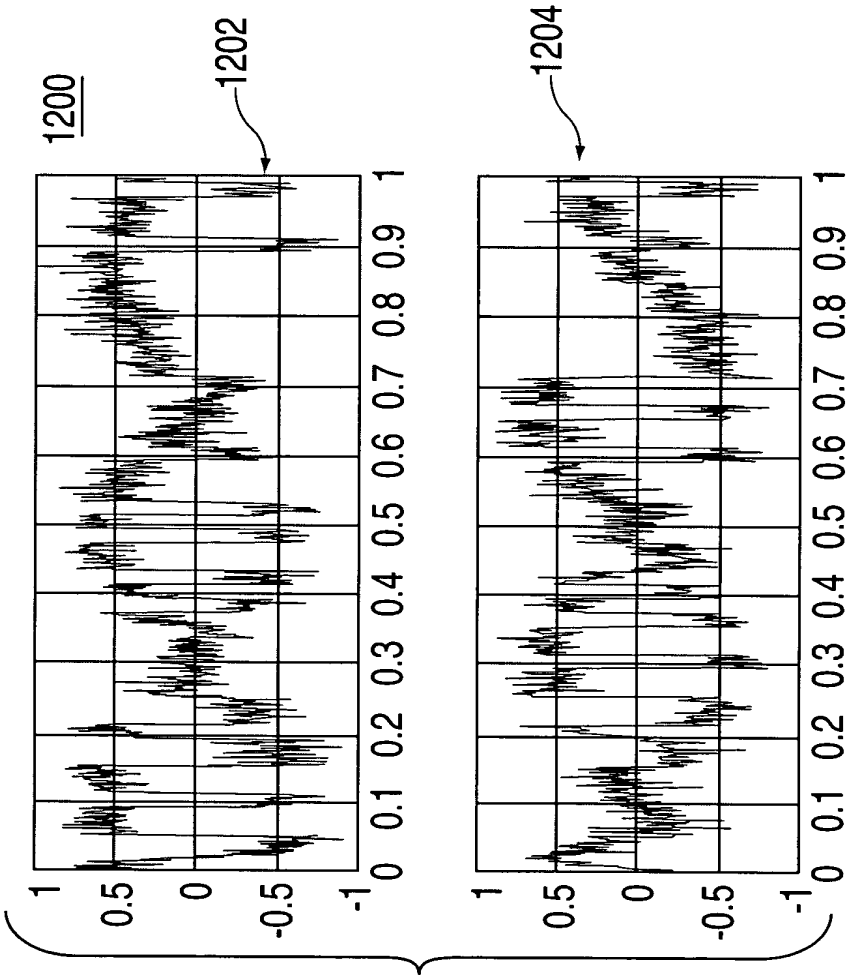

FIG. 12

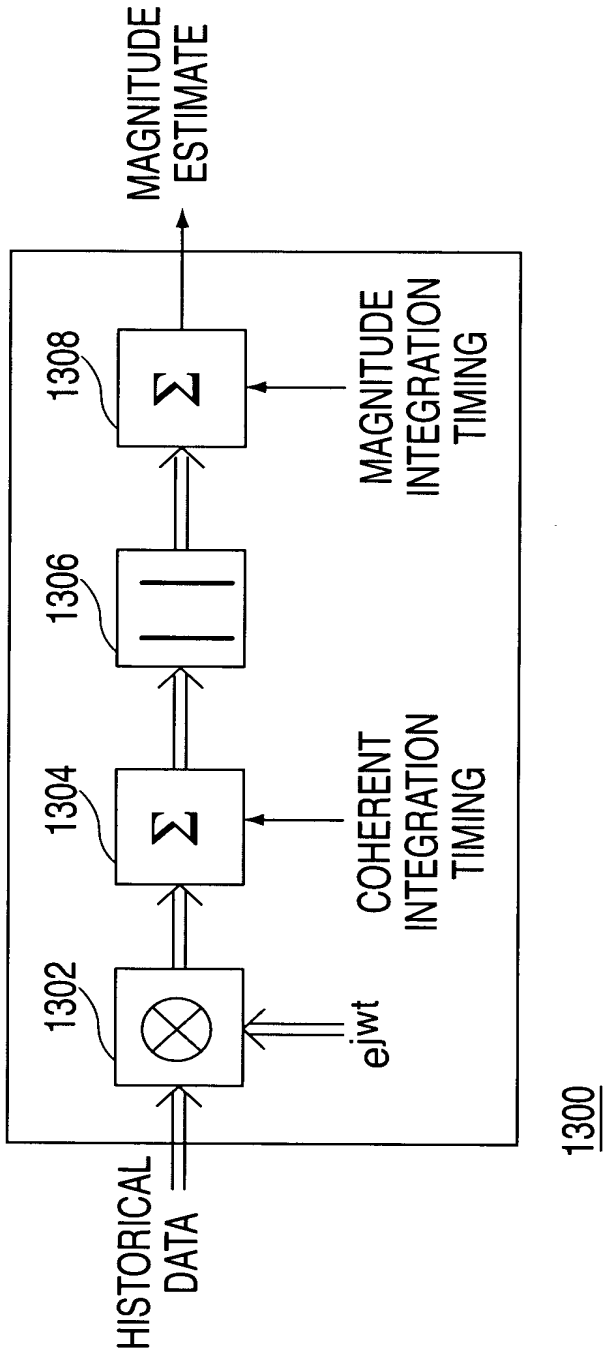
MAGNITUDE ESTIMATE
1308
Σ
MAGNITUDE INTEGRATION TIMING
1306
1304
Σ
COHERENT INTEGRATION TIMING
1302
ejwt
HISTORICAL DATA
1300

FIG. 13

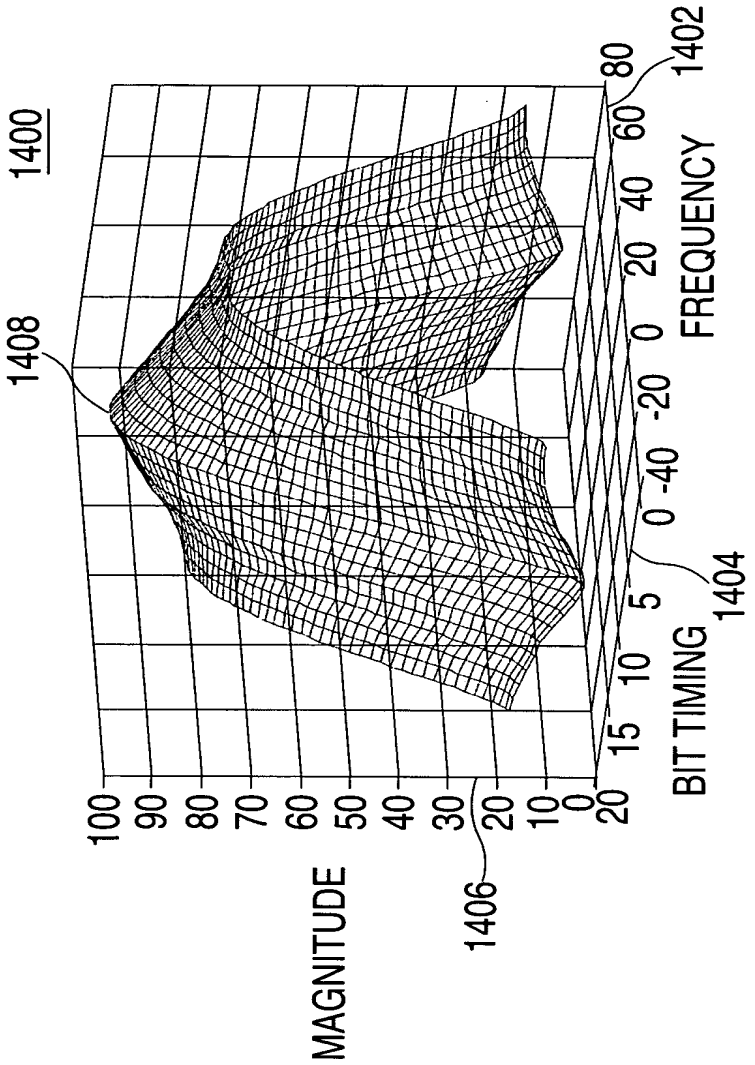
1400
1402
1404
1406
1408
MAGNITUDE
BIT TIMING
FREQUENCY
100
90
80
70
60
50
40
30
20
10
0
20
15
10
5
0
-40
-20
0
20
40
60
80

FIG. 14

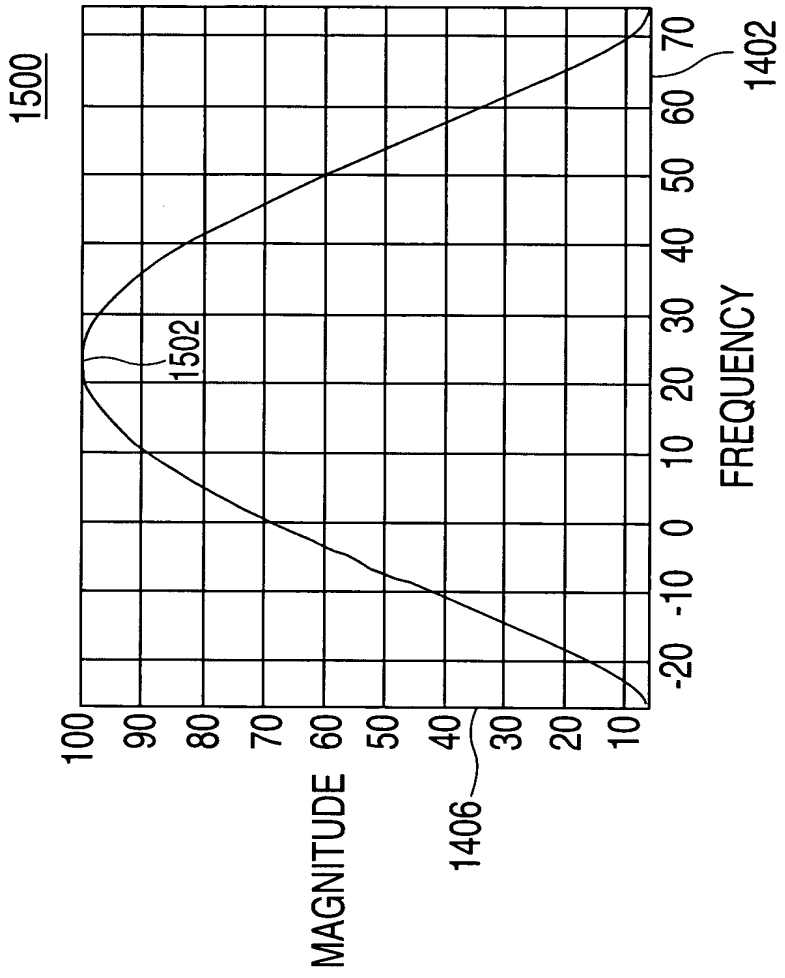
1500
1502
1402
1406
FREQUENCY
MAGNITUDE
-20 -10 0 10 20 30 40 50 60 70
100 90 80 70 60 50 40 30 20 10

FIG. 15

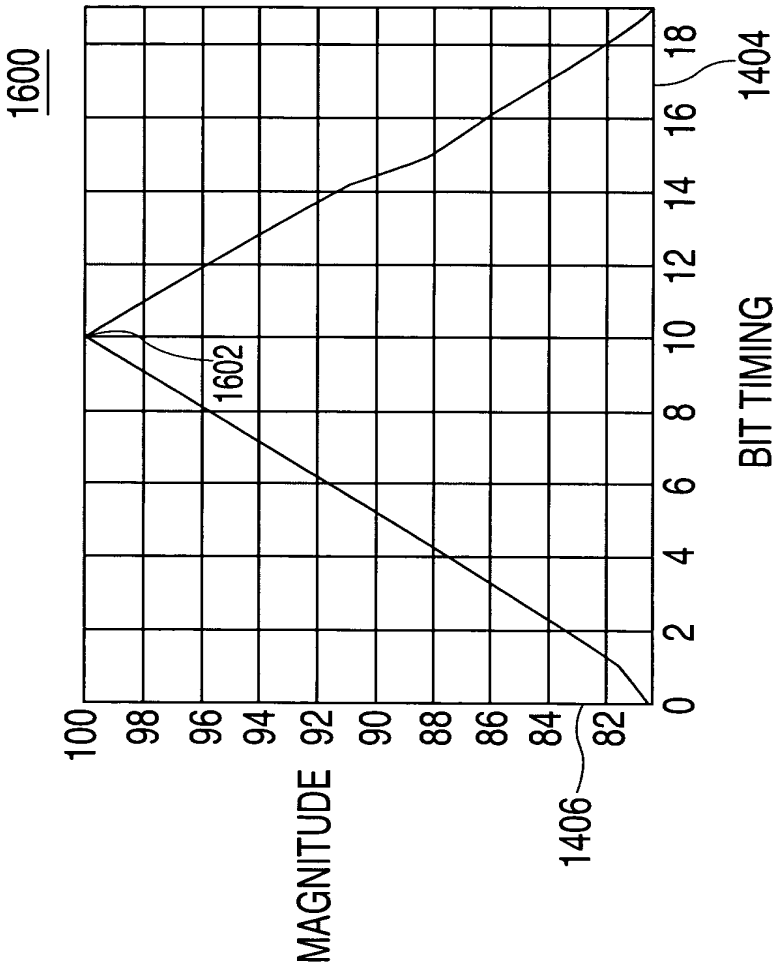
1600
1602
1404
1406
MAGNITUDE
BIT TIMING
100
98
96
94
92
90
88
86
84
82
0
2
4
6
8
10
12
14
16
18

FIG. 16

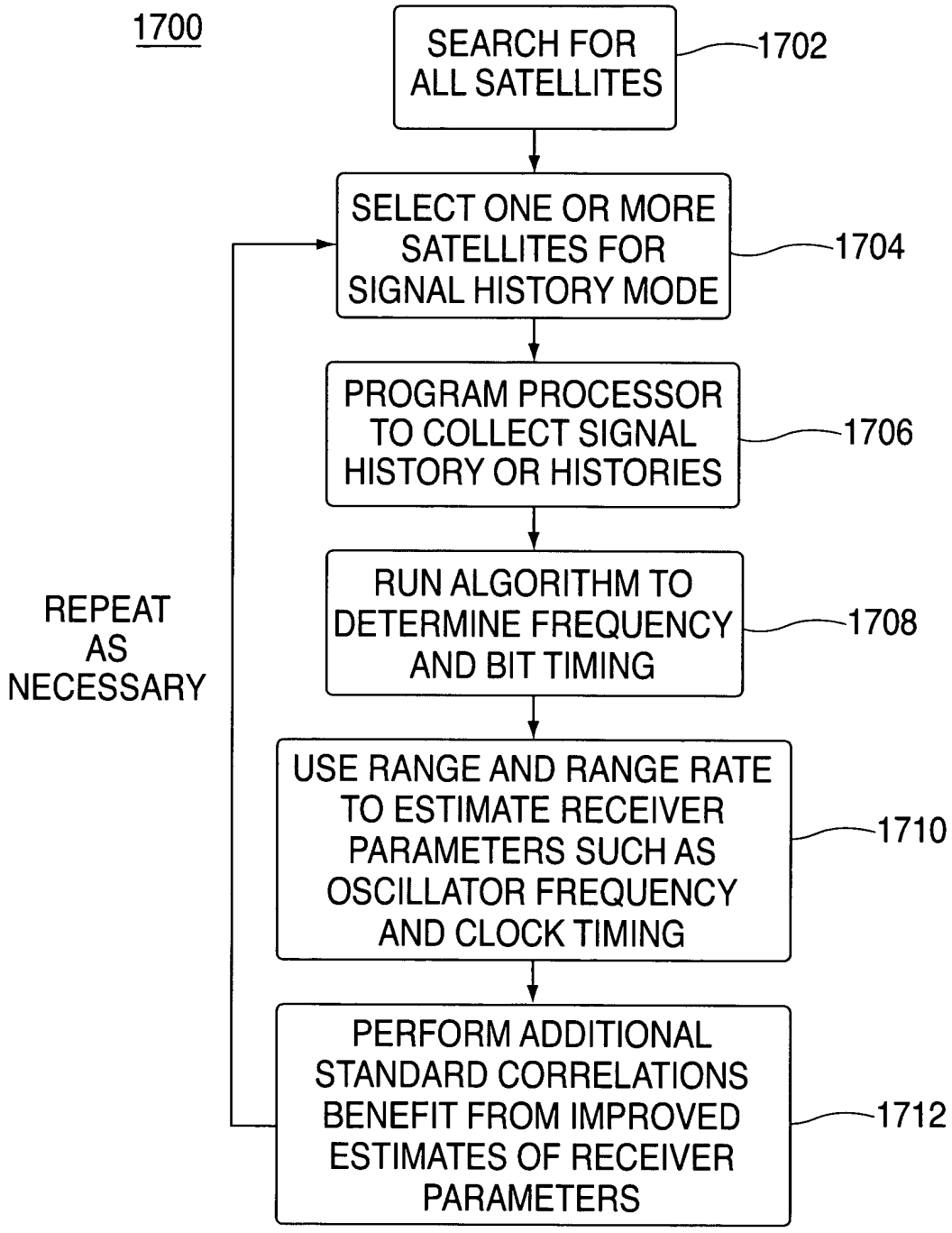
1700
SEARCH FOR ALL SATELLITES
1702
SELECT ONE OR MORE SATELLITES FOR SIGNAL HISTORY MODE
1704
PROGRAM PROCESSOR TO COLLECT SIGNAL HISTORY OR HISTORIES
1706
RUN ALGORITHM TO DETERMINE FREQUENCY AND BIT TIMING
1708
REPEAT AS NECESSARY
USE RANGE AND RANGE RATE TO ESTIMATE RECEIVER PARAMETERS SUCH AS OSCILLATOR FREQUENCY AND CLOCK TIMING
1710
PERFORM ADDITIONAL STANDARD CORRELATIONS BENEFIT FROM IMPROVED ESTIMATES OF RECEIVER PARAMETERS
1712

FIG. 17

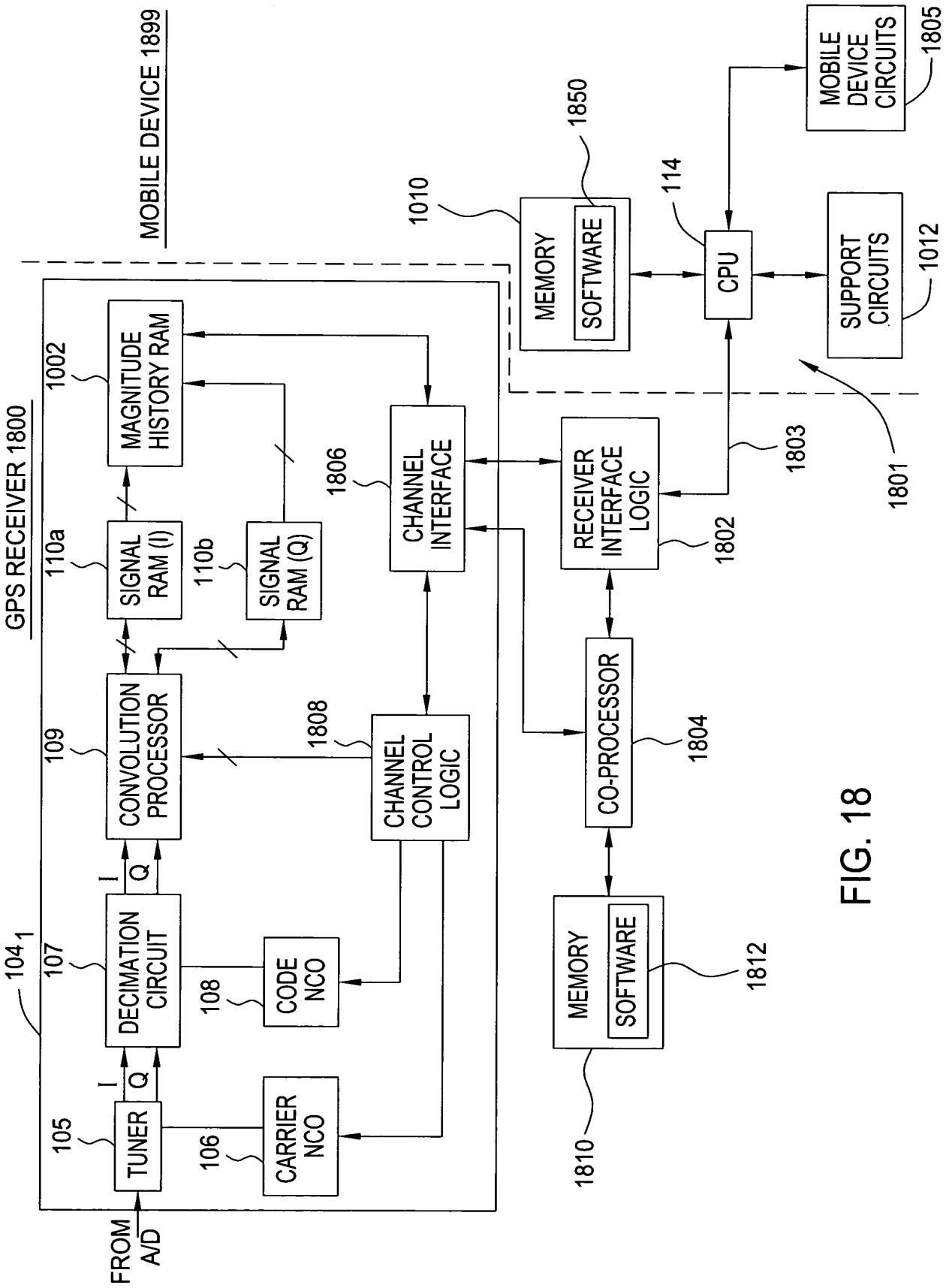
MOBILE DEVICE 1899
GPS RECEIVER 1800
FROM A/D
TUNER
105
DECIMATION CIRCUIT
107
CONVOLUTION PROCESSOR
109
SIGNAL RAM (I)
110a
SIGNAL RAM (Q)
110b
MAGNITUDE HISTORY RAM
1002
CODE NCO
108
CARRIER NCO
106
I
Q
104 1
CHANNEL CONTROL LOGIC
1808
CHANNEL INTERFACE
1806
RECEIVER INTERFACE LOGIC
1802
1803
1801
CO-PROCESSOR
1804
MEMORY
SOFTWARE
1810
1812
1010
MEMORY
SOFTWARE
1850
CPU
114
SUPPORT CIRCUITS
1012
MOBILE DEVICE CIRCUITS
1805

FIG. 18

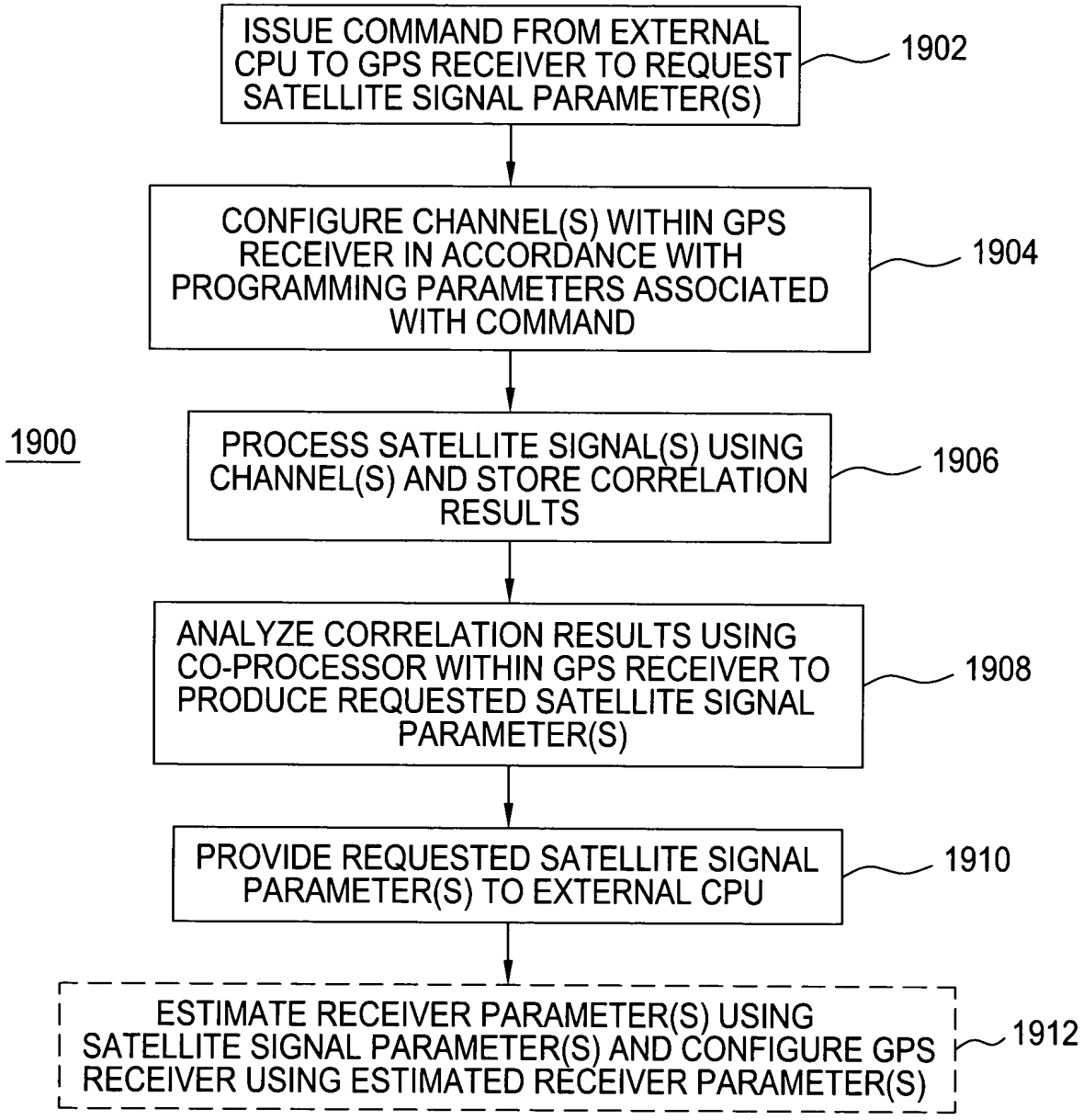
ISSUE COMMAND FROM EXTERNAL CPU TO GPS RECEIVER TO REQUEST SATELLITE SIGNAL PARAMETER(S)
1902
CONFIGURE CHANNEL(S) WITHIN GPS RECEIVER IN ACCORDANCE WITH PROGRAMMING PARAMETERS ASSOCIATED WITH COMMAND
1904
1900
PROCESS SATELLITE SIGNAL(S) USING CHANNEL(S) AND STORE CORRELATION RESULTS
1906
ANALYZE CORRELATION RESULTS USING CO-PROCESSOR WITHIN GPS RECEIVER TO PRODUCE REQUESTED SATELLITE SIGNAL PARAMETER(S)
1908
PROVIDE REQUESTED SATELLITE SIGNAL PARAMETER(S) TO EXTERNAL CPU
1910
ESTIMATE RECEIVER PARAMETER(S) USING SATELLITE SIGNAL PARAMETER(S) AND CONFIGURE GPS RECEIVER USING ESTIMATED RECEIVER PARAMETER(S)
1912

FIG. 19

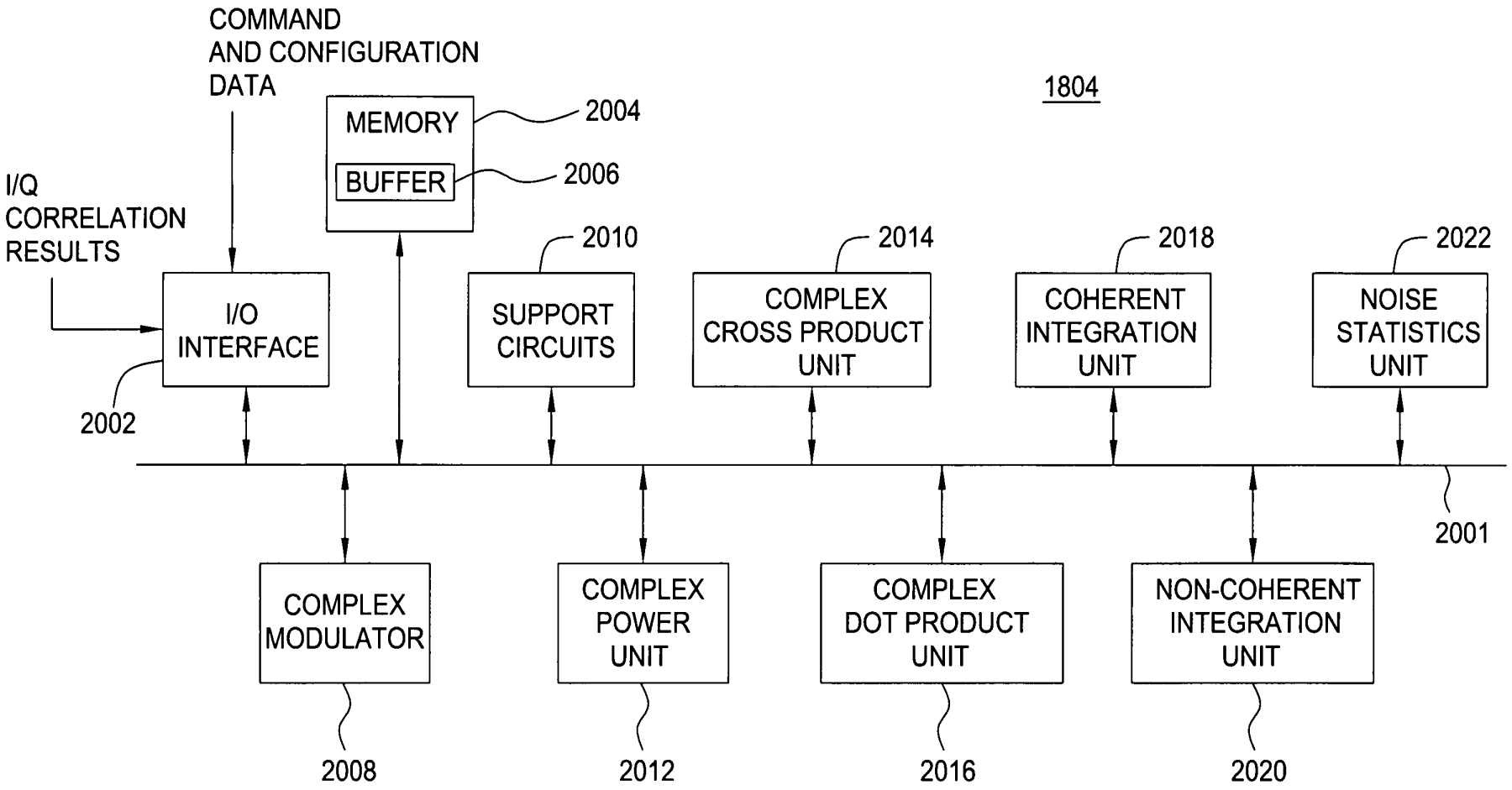
COMMAND
AND CONFIGURATION
DATA
1804
MEMORY
2004
BUFFER
2006
I/Q
CORRELATION
RESULTS
I/O
INTERFACE
2002
SUPPORT
CIRCUITS
2010
COMPLEX
CROSS PRODUCT
UNIT
2014
COHERENT
INTEGRATION
UNIT
2018
NOISE
STATISTICS
UNIT
2022
2001
COMPLEX
MODULATOR
2008
COMPLEX
POWER
UNIT
2012
COMPLEX
DOT PRODUCT
UNIT
2016
NON-COHERENT
INTEGRATION
UNIT
2020

FIG. 20

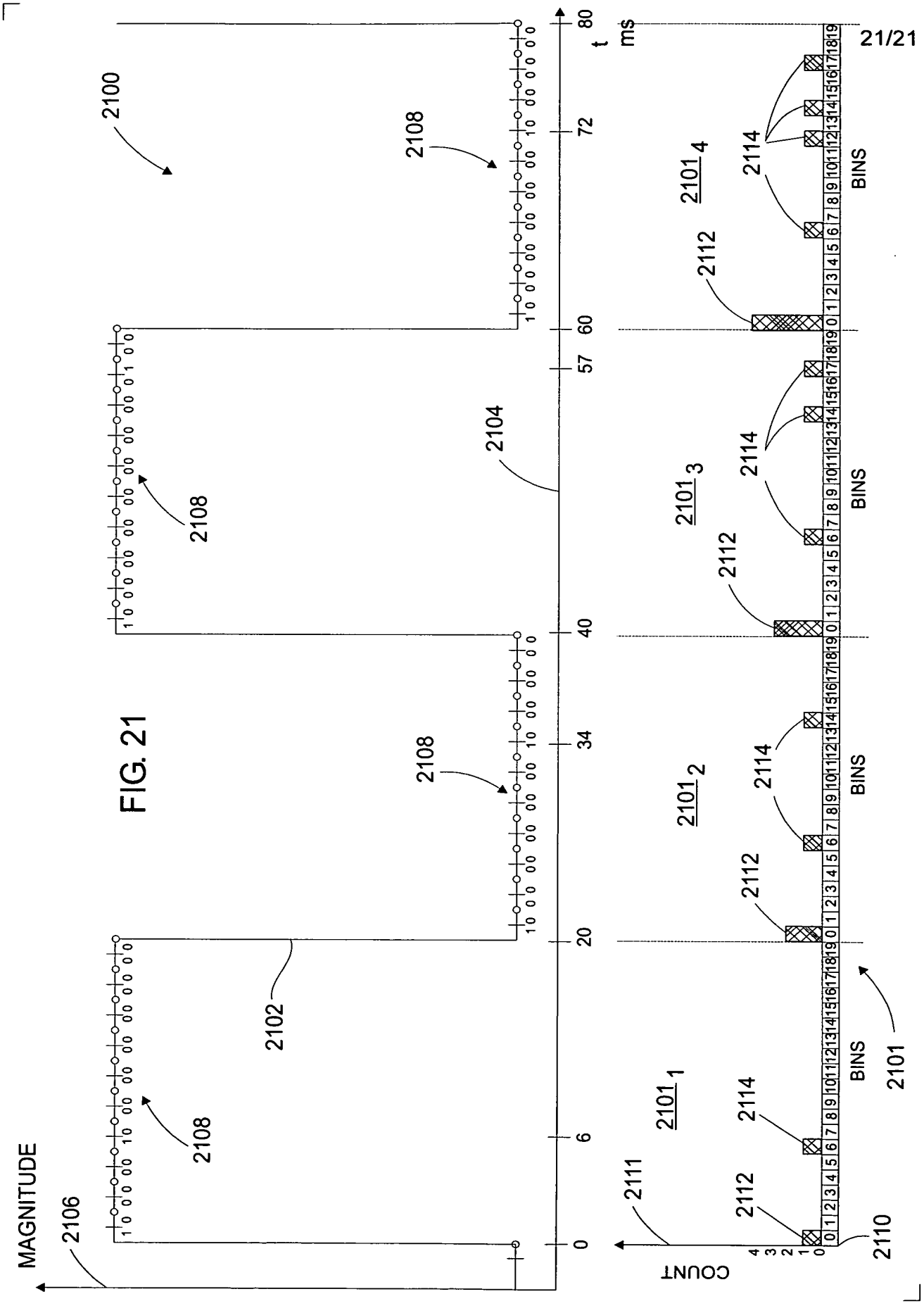
MAGNITUDE
2106
2100
2102
2104
2108
2108
2108
2108
0
6
20
34
40
57
60
72
80
t
ms
2101 1
2101 2
2101 3
2101 4
2101
BINS
2110
2111
2112
2114
COUNT

FIG. 21